Ref: Workshop-4/WECON-CU/2015

Hands-on Workshop on

VLSI Design using Cadence Tools Suite

Workshop objectives:

The aim of this workshop is to provide hands-on experience on the state-of-the-art Cadence EDA tools for VLSI Design. The participants will have an exposure to the Circuit Design & Simulation, Layout, Physical Verification (DRC, LVS), and Extraction. The workshop includes practice sessions on the Cadence design and simulation tools (Encounter, RTL Compiler, Virtuoso, Spectre, Assura and Incisive).

About Cadence

Cadence is a leading provider of EDA and semiconductor IP. Our custom/analog tools help engineers design the transistors, standard cells, and IP blocks that make up SoCs. Our digital tools automate the design and verification of giga-scale, giga-hertz SoCs at the latest semiconductor processing nodes. Our IC packaging and PCB tools permit the design of complete boards and subsystems. Cadence also offers a growing portfolio of design IP and verification IP for memories, interface protocols, analog/mixed-signal components, and specialized processors. And reaching up to the systems level, Cadence offers an integrated suite of hardware/software co-development platforms. In short, Cadence® technology helps customers build great products that connect the world.

Workshop Topics

- Introduction to Cadence and its various tools.
- Basics of mixed signal design using Cadence Virtuoso.
- Introduction to Physical Verification, DRC/LVS by Assura.
- Implementation of NC Launch and RTL Compiler for Digital Circuit using Verilog.
- Extraction of RC Components and Generation of GDSII file.

Resource Person:

- Mr.Vishal Mehta - Design Engineer, Microelectronics and Information Science Research Center
- Ms. KavitaGoswami& Ms. Jasmeen Kaur - Research Assistant, Chitkara University, Punjab

Who can attend?

- UG students working in area of VLSI design
- Researchers (Masters, Doctoral students and Fellows) with thesis in VLSI
- Academicians for enhancing skills in delivering VLSI Labs at Institute/University
- Design engineers from industry

Registration

- Prior registration for the workshop by submitting the duly filled registration form is mandatory before **March 16**. Registration Form & Registration Process is available at Registration Page (CLICK HERE)
- There is a nominal registration fee for attending the workshop. Please visit Registration Page (CLICK HERE) to know the fee structure.
    - There is a special discount on Fee for IEEE & IETE members
- For Conference Authors, workshop registration is absolutely FREE.

Contact

If you have any queries, please contact Mr. Vishal Mehta (vishal.mehta@chitkara.edu.in , 9888836451)