Numerical Simulation of N^+ Source Pocket PIN-GAA-Tunnel FET: Impact of Interface Trap Charges and Temperature

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***Abstract*— This paper investigates the reliability of PIN-gate-all-around (GAA)-tunnel field-effect transistor (TFET) with N^+ source pocket. The reliability of the PNIN-GAA-TFET is examined by analyzing: 1) the impact of interface trap charge (ITC) density and polarity and 2) the temperature affectability on analog/RF performance of the device. It is realized that the interface traps existing at the Si/SiO_2 interface modifies the flatband voltage and, thereby, alters the analog and RF characteristics of the device. The analysis is done at various trap charge densities and polarities. The results, thus, obtained reveal that, at higher trap charge density, the device performance alters significantly. It is obtained that, for a donor trap charge density of 3×10^{12} cm^{-2}, the off-state current of the device degrades tremendously (increases from an order of 10^{-17}–10^{-9}A). The temperature affectability over the device reveals that, at lower gate bias, the Shockley–Read–Hall phenomenon dominates and degrades the subthreshold current of the device at elevated temperatures. However, for the superthreshold regime, the band-to-band tunneling (BTBT) mechanism dominates. Furthermore, the results show enormous degradation in the off-state current at elevated temperatures, such that, with an increase in the ambient temperature from 200 K to 400 K, the I_{OFF} degrades by an order of 10^5, i.e., increases from 10^{-18} A to 10^{-13} A. The results specify that the PNIN-GAA-TFET is insusceptible to the acceptor traps existing at the Si/SiO_2 interface in comparison with the donor traps.**

***Index Terms*— Interface trap charges (ITCs), N^+ source pocket, temperature sensitivity, tunnel FET (TFET).**

I. Introduction

PERPETUAL miniaturization of complementary metal–oxide–semiconductor (CMOS) devices has incredibly revolutionized many areas, such as security, military, mobile communications, and medicine. However, downscaling the CMOS technology results in severe problems, such as high leakage current, high subthreshold swing (SS), and other short channel effects [1]. These challenges enforce for exploring the novel devices that work on new operation mechanisms other than thermionic emission over the thermal barrier as in the case of MOSFET. In this regard, tunnel field-effect transistors (TFETs) that use interband tunneling in the source and channel junction with a control of gate bias has attracted much attention [2]–[6]. The major challenges faced by MOSFET, such as the limitations on the SS that has a fundamental limit of 60 mV/decade and high OFF-state leakage current, have been overcome by TFET up to a great extent. In TFET, the large tunneling barrier width present at the source–channel junction at lower gate bias blocks the tunneling of electrons and, thereby, benefits a very low leakage current. However, the band-to-band tunneling (BTBT) of carriers from the source potentially allows a steep SS values [7]. Apart from these merits, TFET suffers from low ON-current, high threshold voltage (V_{th}), high gate–drain parasitic capacitance, and ambipolar current [8], [9]. For superior analog/RF performance, many device engineering architectures and III–V materials have also been proposed by various researchers [2], [8], [10]–[15]. Among all device engineering architectures, the N^+ source pocket p-i-n TFET or PNIN-TFET proposed by [14] is a strong candidate as it offers higher ON-current with lower SS and lower V_{th}. III–V TFET, however, mitigates the problem of lower I_{ON} offered by their lower bandgap, lower effective mass, and wide range of band alignments; thus, III-V material-based TFETs have the potential of high switching speed, but at the same time suffering from large SS [16]. However, the basic device characteristics, such as improved analog, RF, and linearity of TFET, have been the major encompassing area of the investigation up to now. Recently, Moselund *et al.* [9] fabricated lateral p-type InAs/Si TFET with I_{ON} of a few μA/μm for $|V_{ds}| = |V_{gs}| = 0.5$ V. A SiGe/Si heterostructure TFET has been fabricated by Blaeser *et al.* [17] that shows I_{ON} of 6.7 μA/μm at $V_{dd} = 0.5$ V and SS of ~80 mV/decade. Nonetheless, for sub-100-nm devices, the reliability of TFET is also a critical concern, owing to the strong electric field at the source–channel junction. This strong electric field roots to the generation of defects at the $Si–SiO_2$ interface [18]. Along with the high electric field, the fabrication processes for sub-100-nm devices, such as the plasma etching, may damage the gate oxide and the Si-oxide interface. These defects are the origin of fixed interface and oxide

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