Temperature Associated Reliability Issues of Heterogeneous Gate Dielectric—Gate All Around—Tunnel FET

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***Abstract*—In this paper, the temperature associated reliability issues of heterogeneous gate dielectric-gate all around-tunnel FET (HD GAA TFET) has been addressed, and the results are simultaneously compared with gate all around tunnel FET (GAA TFET). This is done by investigating the effect of interface trap charges such as donor (positive interface charges) and acceptor (negative interface charges) at various operating temperatures on the device analog parameters and RF figure of merits. It is observed that, at high gate bias, TFET exhibits weak temperature dependence owing to the weak dependence of band to band tunneling phenomenon on the temperature in comparison to the large temperature variation for lower gate bias due to the temperature dependence of Shockley-Read-Hall (SRH) phenomenon. Results reveal that extremely high OFF current at elevated temperatures degarades the device performance, making the device less reliable for high-temperature applications. Moreover, at elevated temperature, the decrease in threshold voltage and intrnsic delay, and increase in cut off frequency is found, thereby upgrading the device characteristics. All the simulations have been done on ATLAS device simulator.**

***Index Terms*—Ambipolarity, Digital applications, Gate all around, Hetero gate dielectric (HD), Interface trap charges (ITC), Temperature Sensitivity, Tunnel FET (TFET).**

I. Introduction

UNIQUE properties of tunnel FET (TFET) such as low I_{off}, sub-60 mV/decade subthreshold swing (SS), immunity against short channel effects and its compatibility with the CMOS process makes it a suitable candidate for ultra low power applications [1], [2]. However, the ON-state current in TFET is limited due to the band to band tunneling (BTBT) phenomenon, making it incompatible to meet the increased demand for high speed with low power consumption applications. Many remedies have been proposed to improve the driving current of TFET [3]–[7]. Another shortcoming of TFET is the ambipolar conduction [8]; this can cause severe problems such as malfunction of the inverter-based logic circuits. To overcome these challenges collectively, a Hetero Gate dielectric TFET (HD TFET) was proposed [4], which combines the merits of TFET with high-k material as dielectric (at higher gate bias) and TFET with SiO_2 as dielectric (at lower gate bias). In HD TFET, the local minima formed at the tunneling junction enhance the ON current of TFET whereas; the SiO_2 placed over the drain-channel junction mitigate the ambipolar behavior of TFET.

Till now, mainly the device performance has been studied for various novel device architectures and material engineering of TFET to improve the device performance, but to consider the device reliability and applicability for wide range temperature applications, the temperature affectability as well as interface trap charges (ITC) must be analyzed. Moreover, it has been reported that the reliability of TFET is more prominent problem due to the change in tunneling field induced by ITCs, in comparison with MOSFET [9].

In case of tunnel FET, higher electric field near the tunneling junction (the source-channel junction) is desired for lowering of the tunneling barrier width, but on the contrary, this high transverse field results into the generation of interface traps (donor and acceptor) and hence the localized charges (both positive and negative). These trap charges can cause severe issues on device reliability and lifetime of the device [10]. As reported previously, the amalgamation of HD scheme on TFET significantly improves the analog [2] and RF performance [11] of the device. However, the on-chip performance of the device is always subject to the operating temperature. The increased number of transistors on the chip enhances the heat dissipation and thus raises the operating temperature of the chip and the device significantly. Also, as the properties of the semiconductor are also dependent on temperature, thus, there is a need to study the effect of temperature in order to investigate the stability of the device [12], [13]. Moreover, from the perspective of application of transistors in some extreme conditions (where the operating temperature is different from the nominal room temperature) such as the furnace temperature control, satellite communications, military, medical equipment, aerospace, automobile, nuclear sectors, wireless/mobile communications, it is important to investigate the device behaviour at a wide range of temperatures.

The core aim of this script is to fulfill the above desires, i.e. the need to investigate the reliability concern of TFET subjective to the impact of operating temperature and effect of the ITCs (owing to the fact of fabrication process damages). This is done

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