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Impact of metal silicide source electrode on polarity gate induced source in junctionless TFET

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Abstract
Tunnel Field Effect Transistors (TFET) based on quantum mechanical band to band tunneling (BTBT) are promising alternatives for low power analog applications. Additionally, the concept of junctionless (JL) devices realized by the charge plasma concept offers added advantages in terms of simplified fabrication techniques. In n type JL-TFET, p+ source is induced using a polarity gate (PG) with suitable work function. However, retention of induced p+ source is not a sole contribution of PG, the source electrode (SE) metal silicide work function also plays a significant role in the retention of hole plasma (specially near the interface of SE/induced source). Thorough study regarding the combined influence of PG and SE metal silicide work function on induced p+ source is missing in the literatures. This work explores the performance of JL-TFET of different SE metal silicide such as $TiSi_2$ (4.53 eV), $CrSi_2$ (4.85 eV) and Pd_2Si (5.3 eV). It is perceived that for SE metal silicide with work function lower than p+ induced source i.e., $TiSi_2$ and $CrSi_2$ the depletion of hole plasma (formation of Schottky interface) appears near the SE/p+ induced source interface. The depletion of hole plasma is attributed to the combined electric field of SE metal silicide and the PG, the immediate consequence is the refrainment of current. Further, due to the formation of Schottky interface for $TiSi_2$ and $CrSi_2$, the performance of the device is examined by revoking and evoking the Universal Schottky Tunneling (UST) model. Results reveal the undervalued performance of the device without the inclusion of UST, primarily a lower drain current (and thereby the analog performance) of the device is obtained, since it ignores the Schottky tunneling at SE/p+ induced source interface. However, the inclusion of UST model emulates the performance of JL-TFET precisely, by incorporating the Schottky tunneling at the SE/p+ induced source interface. Thus, for the retention of hole plasma, appropriate SE work function i.e., $\Phi_{SE} > \Phi_{p+\text{ induced source}}$ is required, whereas for SE work function $\Phi_{SE} < \Phi_{p+\text{ induced source}}$ appropriate Schottky tunneling must be considered for accurate analysis of the device. The study also reveals that the depletion of hole plasma and hence the formation of Schottky interface can be avoided using SE with metal work function source for which consideration of UST is immaterial.

1 Introduction

Huge growth in applications such as 5G, Internet of Things, big data analytics, cloud computing and artificial intelligence have increased the demand of most prompt electronic devices like never before. These next generation devices are expected to respond and act favourably to the clock frequencies as high as few GHz. While conventional devices such as nMOS, pMOS, combination of the two i.e., CMOS, or other forms of the same such as High Electron Mobility Transistor (HEMT), BiCMOS and Heterojunction Bipolar Transistor (HBT) have been more or less meeting the requirements of these technological changes, but their performance falters at the sub 20 nm technology node. Though the continuous scaling down of CMOS technology from last few decades has enhanced the packing density and operation speed, however,

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