Low-Voltage Low-power Bulk-Driven and Bulk-driven-quasi-floating-gate neural amplifier design for EEG

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Abstract. This paper focuses on the usage of non-conventional techniques viz. Bulk-driven (BD) and Bulk-driven-quasi-floating-gate (BDQFG) to design low-voltage (LV) and low-power (LP) pre-amplifier for electroencephalogram (EEG). Gate–Driven (GD) Three-Current-Mirror Operational Trans-conductance Amplifier (OTA) is compared with BD-OTA and BDQFG-OTA. The efficient g_m/I_D methodology is used to set the aspect ratios of the MOSFETs used in three topologies which are structured in 0.18 µm CMOS technology node using BSIM3V3 MOS Transistor Model from Cadence. The simulation results display that the non-conventional techniques attain the gain of 39.62dB (BD-OTA) and 39.33 dB (BDQFG-OTA) while reducing the power consumption by 45% in comparison to GD-OTA. The BD-OTA operates at ±750mV voltage supply, and power consumption is 314nW while BDQFG-OTA works at ±1.1 V voltage supply, and power consumption is 377nW attaining the similar performance parameters as GD-OTA.

Keywords: Operational Trans-conductance Amplifier, EEG, g_m/I_D method, Bulk-Driven, Gate-Driven, BDQFG

1 Introduction

Electroencephalograph (EEG) is a standard neural bio-potential signal which is recorded regularly in contemporary medical practice. This minuscule signal is acquired using non-invasive electrodes (with jelly or active) which are in contact with the skin on the skull. EEG has an average signal magnitude of 1µV to 100µV occupied in the frequency band from a fraction of 1Hz to approximately 100Hz [1-3]. Enhanced understanding of these signals aids the engineers in designing better prosthetics for the specially-abled persons, with a purpose to improve patients' quality of life without any hindrance due to size, weight, wired power connection of these devices [2,3]. The extended applications of improved EEG acquisition could be in sporting, entertainment (gaming), comfort monitoring, disease analysis, and so on.

The advancement in NEMS/MEMS technology has made it possible to increase the density of the electrodes for the better-quality acquisition of EEG [3]. Thus, a robust analog front end is required to amplify and digitise these signals without corrupting the signal due to the presence of circuit nonlinearities and electronic noise. Low power, lesser area and low noise are the key characteristics required for an illustrative analog front end (AFE) system shown in Fig. 1. E_1 and E_2 represent two parallel EEG electrodes, followed by a neural amplifier (first stage), which plays a vital role in achieving the required power and noise performance of the entire system. Consequently, the differential amplification at this stage is achieved using Operational Trans-conductance Amplifier (OTA), most frequently used analog circuit for neural amplifier design [1-3].

The design specifications of OTA are dictated by the EEG signal characteristics and the electrical characteristics of the electrodes. The electrodes are modelled as a parallel combination of resistors and capacitor with high impedance value of the order of mega ohm [1, 3]. A low-frequency offset voltage signal which exists due to the artefacts between the electrode and skin contact is added to the desired EEG signal. Therefore, the desirable features of OTA are high input impedance, limited bandwidth, acceptable gain, high common mode rejection ratio (CMRR), high power supply rejection ratio (PSRR), minimum input referred noise and low Noise Efficiency factor (NEF) [4,5]. This paper focuses on low voltage (LV) and low power (LP) design of Three-Current-Mirror OTA while maintaining the trade-off between the characteristics as mentioned above [4].

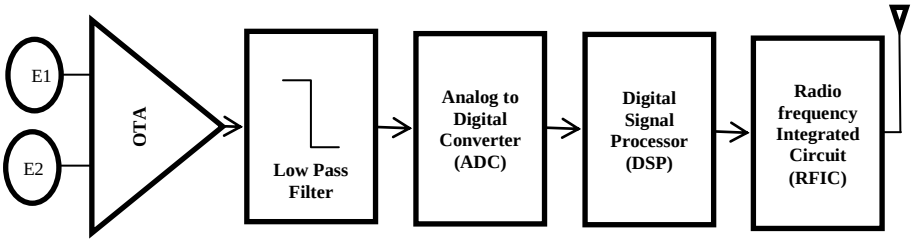

Fig.1. Typical Analog Front End System (AFE)

The researchers have deliberated LV-LP operation using both conventional [1,2,3,6,7,9,14] and non-conventional techniques [4,5,9,11,12,13,15]. Reported conventional techniques for power reduction are the reducing bias current [9], the operation of MOSFET in weak inversion [6,7], improvement in design by adding current stealing branches [8,9,14], rail-to-rail operation and so on. However, the non-conventional techniques are focused on the reduction of the threshold voltage or even the elimination of the same achieved by Floating gate (FG) approach [4, 11], Bulk-driven (BD) MOSFETs [12, 13], Quasi-Floating-Gate (QFG) approach and Bulk-driven-quasi-floating-gate (BDQFG) MOSFET [11-13, 15]. In this paper, the design of OTA for a neural amplifier using Gate-driven (GD), Bulk-driven (BD) and BDQFG is proposed to meet the design requirements mentioned in Table-1. The dimensions of various MOSFETs were decided using g_m/I_D methodology which addressed the challenges in the construction of low power, small area and low noise three-current-mirror OTA using GD, BD and BDQFG approach specific for the EEG recordings [6, 7]. All experimentations of the proposed designs were simulated using