G_m/I_D method based low-power, low-noise Pre-amplifier design for EEG

[1]Lipika Gupta, [2]Amod Kumar, [1]Sartajvir Singh
[1]ChitkaraUniversity, Himachal Pradesh
[2]National Institute of Technical Teachers Training and Research, Chandigarh

Abstract: This paper presents the design of pre-amplifier for electroencephalogram (EEG) measurement using efficient g_m/I_D methodology. Graphical representation using tradeoff-charts are used to meet the target specifications and decide device dimensions for Three-Current-Mirror Operational Trans-Conductance Amplifier (OTA) topology used in Pre-amplifier. While concentrating on low-power and low-noise design, the pre-amplifier is structured in 0.18 µm CMOS technology using Cadence Spectre. The simulation results show that the designed pre-amplifier display the gain of 47.62 dB, Bandwidth of 0.002-3.5 kHz, integrated input-referred noise voltage is 5.28 µVrms, NEF=1.627, CMRR ≥ 84 dB and PSRR ≥ 80 dB. The power utilization of the pre-amplifier is equal to 833nW. The post-layout simulation results show the gain deviation of 2.7% due to parasitic.

Keywords: Operational Trans-conductance Amplifier, EEG, g_m/I_D method, Pre-amplifier

I. INTRODUCTION

Neurons speak with one another and create neural signs which can be utilized to break down the cerebrum movement. The fastidious checking of these signs upheld by present-day IC innovation can empower people in the secured position to use different prosthetic gadgets successfully. A few intrusive strategies, for example, electrocorticography (ECoG) include the position of electrically-conductive sharp microelectrodes lying on the cerebrum tissue are performed inside the body. However, the most ordinarily utilized non-intrusive strategy to record neural movement by setting cathodes on the scalp is Electroencephalography (EEG) (1µV to 100mV). Pre-amplifier is the first stage of the EEG amplifier which is utilized to amplify exceptionally low recurrence mind signals [1].

Neural signals are obtained using dry or active electrodes which are connected at the input of pre-amplifier. To structure preamplifier, Operational Trans-conductance Amplifier (OTA) is the most important circuit for better execution and furthermore for a power-concentrated circuit [1, 2]. The OTA should be steady and should gather undistorted EEG signal rejecting the offset voltage induced due to the interface between the terminal and the tissue. This paper discusses the design of the preamplifier for the purpose of amplifying EEG recordings where focused design considerations are low power consumption, lesser area, low noise, high CMRR & high PSRR.

Harrison and Charles [2] accomplished better Noise efficiency factor (NEF) at the expense of power and high bias current. The schematic of the same pre-amplifier is shown in Figure 1(a) and three-current-mirror topology shown in Figure 1(b) [2]. The proper transistor sizes profoundly influence the power and noise specifications. Therefore, a strategic technique is required to decide the device dimensions while targeting the required design specifications [3]. The standard square law equations cannot be used for defining the MOSFET dimensions because operating in strong inversion increase the power budget. For Low power and Low noise operation, the required region of operation for transistors is moderate inversion region and/or weak or sub-threshold region [3, 4].

EKV models or BSIM Models exploit the equations of current in weak and moderate regions. These models use complicated equations for obtaining device dimension which cannot be used for traditional hand estimations. The divergence between present-day CMOS models and customary square law equations because of the dependence on ineffectively characterized parameters such as μC_{OX}, V_{th}, V_{dsat}, etc., pose a challenge in meeting the design specifications for analog circuits. The g_m/I_D methodology crosses over any barrier between the hand calculations and simulations obtained from circuit simulator [4].

Inaccurate simple models are replaced by the datasets generated by the simulation sweeps for different values of Length. Normalized transistor parameters Vs g_m/I_D, Figure of Merit Vs g_m/I_D plots are obtained to obtain the optimized values of W/L. The idea of using g_m/I_D as primary design variable is advocated by the fact that it is a normalized measure of the channel inversion level for all operating regions [4, 5]. Besides, once the data set generated for g_m/I_D for a given technology, it can be used again in the form of lookup tables and further simplifies the design procedure.

This paper demonstrates g_m/I_D methodology [3, 4, 5] to address the challenges in construction low power; small area and low noise current mirror OTA design for optimizing device dimensions of MOSFETs in the OTA, specific for the EEG recordings. The proposed design is simulated using the 0.18µm technology node using BSIM3V3 MOS Transistor Model from Cadence Spectre. Section II presents the g_m/I_D method to select the aspect ratios of transistors in Current mirror OTA, Section III deliberates the results obtained from the sizing and provides the comparison with the existing literature, Section IV presents the pre and post-layout simulation results, and finally, the conclusion summarizes the acquired results.